AMENDMENTS TO THE CLAIMS:

Please cancel claims 1-17 and Add the following new claims 18-28 as follows:

18. (Added): Apparatus for converting an M-bit digital signal into an analogue signal, the apparatus comprising:

means for mapping the M-bit digital signal to first and second digital values u and v, so that the ratio of u/v to the maximum value of u/v is equal to or approximates the ratio of the M-bit digital signal to the maximum value of that signal;

first and second digital to analogue converters, the first digital to analogue converter having an input for receiving said first digital value and the second digital to analogue converter having an input for receiving said second digital value; and

circuit means coupled to the analogue outputs of the digital to analogue converters for diving one of the analogue outputs by the other, and for providing the result to an output.

19. (Added): Apparatus according to claim 18, wherein the bit length N of the first digital value u is the same as that of the second digital value v.

20. (Added): Apparatus according to claim 18, wherein said means for mapping comprises a memory storing a look-up table, the look-up table containing all possible values of said M-bit digital signal and respective first and second value pairs u,v.

21. (Added): Apparatus according to claim 19, wherein said means for mapping comprises a memory storing a look-up table, the look-up table containing all possible values of said M-bit digital signal and respective first and second value pairs u,v.

22. (Added): Apparatus according claim 18, wherein the means for mapping comprises means for compressing said M-hit digital signal by a factor A, said circuit means comprising means for scaling the result of said division by the same factor A.

23. (Added): Apparatus according to claim 20, wherein the means for mapping comprises means for compressing said M-hit digital signal by a factor A, said circuit means comprising means for scaling the result of said division by the same factor A.

24. (Added): Apparatus according to claim 21, wherein the means for mapping comprises means for compressing said M-hit digital signal by a factor A, said circuit means comprising means for scaling the result of said division by the same factor A.

25. (Added): A method of converting an M-bit digital signal into an analogue signal, the method comprising:

mapping the M-bit digital signal to first and second digital values u and v, so that the ration of u/v to the maximum value of u/v is equal to or approximates the ration of the M-bit digital signal to the maximum value of that signal;

applying said first and second digital values to inputs of the first and second digital to analogue converters respectively; and

dividing the analogue output of one of the digital to analogue converters by the other, and providing the result to an output.

26. (Added): Apparatus which is configurable to evaluate a function, the apparatus comprising:

a plurality of scaling elements, each scaling element having a first input for receiving an analogue input signal, a second input, and an output;

control means for generating a digital weight for one or more of said scaling elements, and having output means for applying generated weights to the second inputs of respective scaling elements;

Output means having a plurality of inputs coupled to outputs of respective scaling elements to receive scaling products therefrom, a plurality of outputs selectively coupled to respective inputs, and means for selectively coupling inputs or outputs together, the control means being coupled to the output means for effecting the selective coupling.

27. (Added): Apparatus according to claim 26, wherein said scaling elements are multiplication elements, division elements, or elements configurable to perform either multiplication or division.

28. (Added): Apparatus according to claim 27, wherein said scaling elements are multiplying digital to analogue converters.

29. (Added): Apparatus according to claim 26, wherein the apparatus is configurable to operation as a vector dot product multiplier.

30. (Added): Apparatus according to claim 27, wherein the apparatus is configurable to operation as a vector dot product multiplier.

31. (Added): Apparatus according to claim 28, wherein the apparatus is configurable to operation as a vector dot product multiplier.